



# STP3NC70Z STP3NC70ZFP

## N-CHANNEL 700V - 4.1Ω - 2.5A TO-220/TO-220FP Zener-Protected PowerMESH™III MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP3NC70Z	700V	< 4.7Ω	2.5 A
STP3NC70ZFP	700V	< 4.7Ω	2.5 A

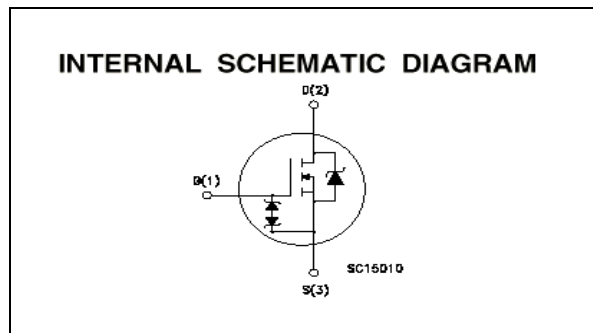
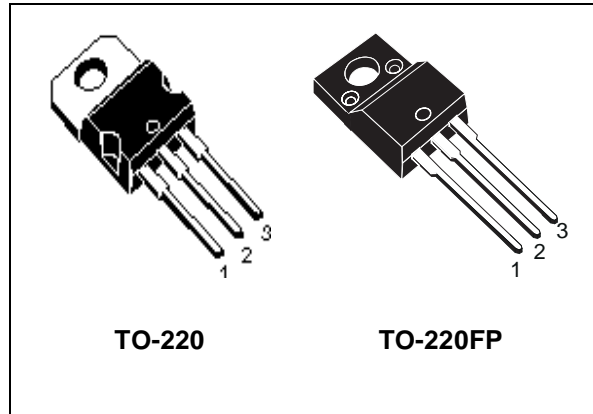
- TYPICAL R<sub>DS(on)</sub> = 4.1Ω
- EXTREMELY HIGH dv/dt AND CAPABILITY GATE TO - SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW GATE INPUT RESISTANCE
- GATE CHARGE MINIMIZED

### DESCRIPTION

The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

### APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP3NC70Z	STP3NC70ZFP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	700		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	700		V
V <sub>GS</sub>	Gate- source Voltage	± 25		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	2.5	2.5 (*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	1.6	1.6 (*)	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	10	10	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	65	35	W
	Derating Factor	0.52	0.28	W/°C
I <sub>GS</sub>	Gate-source Current (DC)	±50		mA
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	1.5		KV
dv/dt (1)	Peak Diode Recovery voltage slope	3		V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	-	2500	V
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature	150		°C

(●) Pulse width limited by safe operating area  
June 2001

(1) I<sub>SD</sub> ≤ 2.5A, di/dt ≤ 100A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

(\*) Limited by Maximum Temperature allowed

## STP3NC70Z/STP3NC70ZFP

### THERMAL DATA

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	1.92	3.57	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	2.5	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	150	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	700			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0		0.8		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V			±10	μA

#### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.25 A		4.1	4.7	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 1.25A		2		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		530		pF
C <sub>OSS</sub>	Output Capacitance			50		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			7		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)****SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 350\text{ V}$ , $I_D = 1.25\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		14		ns
$t_r$	Rise Time			11		ns
$Q_g$	Total Gate Charge	$V_{DD} = 560\text{ V}$ , $I_D = 2.5\text{ A}$ , $V_{GS} = 10\text{ V}$		17	24	nC
$Q_{gs}$	Gate-Source Charge			4		nC
$Q_{gd}$	Gate-Drain Charge			7		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 560\text{ V}$ , $I_D = 2.5\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		16		ns
$t_f$	Fall Time			33		ns
$t_c$	Cross-over Time			40		ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				2.5	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				10	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 2.5\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 2.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 27\text{ V}$ , $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		175		ns
$Q_{rr}$	Reverse Recovery Charge			0.6		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			7.5		A

**GATE-SOURCE ZENER DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{ mA}$ (Open Drain)	25			V
$\alpha_T$	Voltage Thermal Coefficient	$T = 25^\circ\text{C}$ Note(3)		1.3		$10^{-4}/^\circ\text{C}$
$R_z$	Dynamic Resistance	$I_D = 50\text{ mA}$ , $V_{GS} = 0$		90		$\Omega$

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

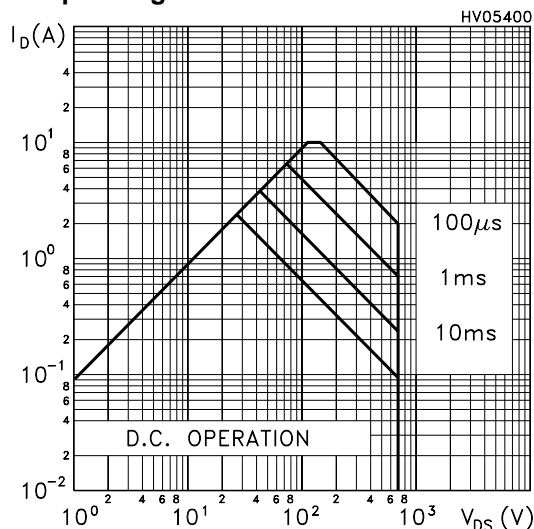
2. Pulse width limited by safe operating area.

3.  $\Delta V_{BV} = \alpha_T (25^\circ - T) BV_{GSO}(25^\circ)$

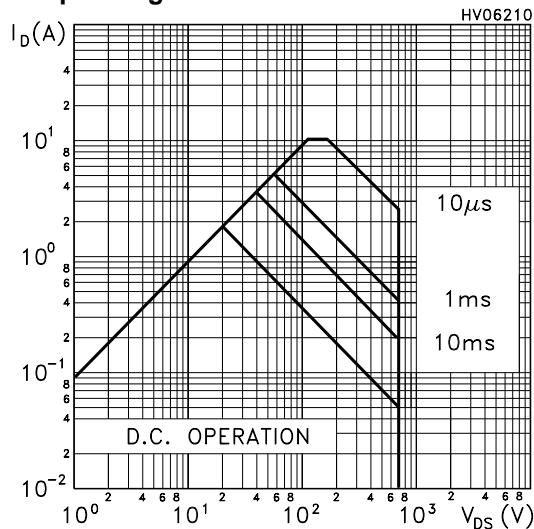
**PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES**

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the 25V Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

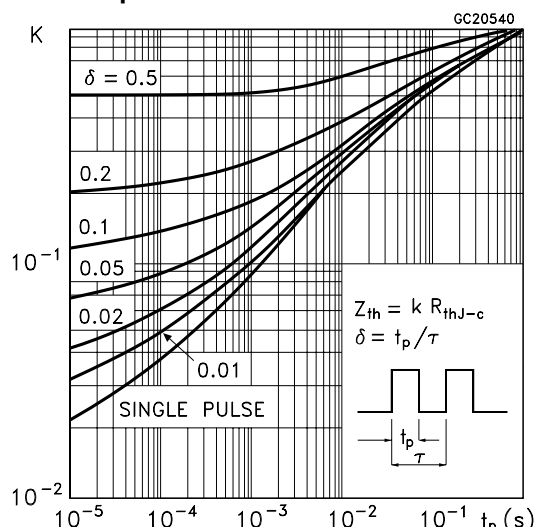
Safe Operating Area for TO-220



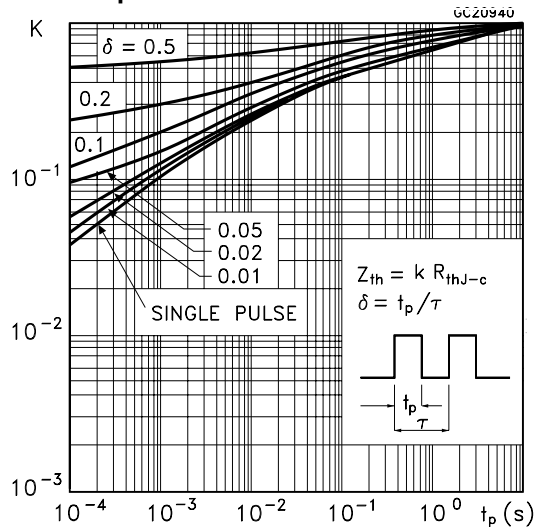
Safe Operating Area for TO-220FP



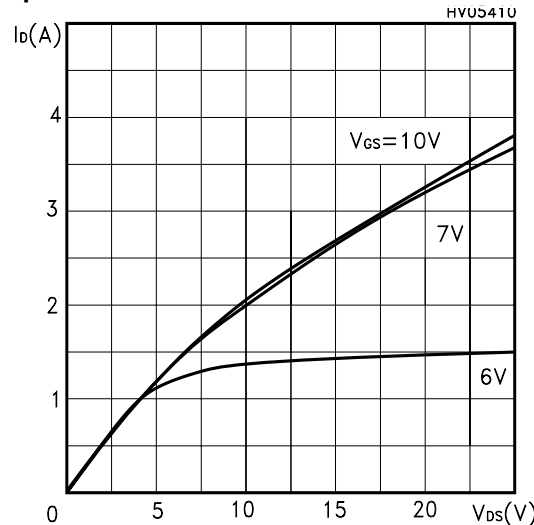
Thermal Impedance for TO-220



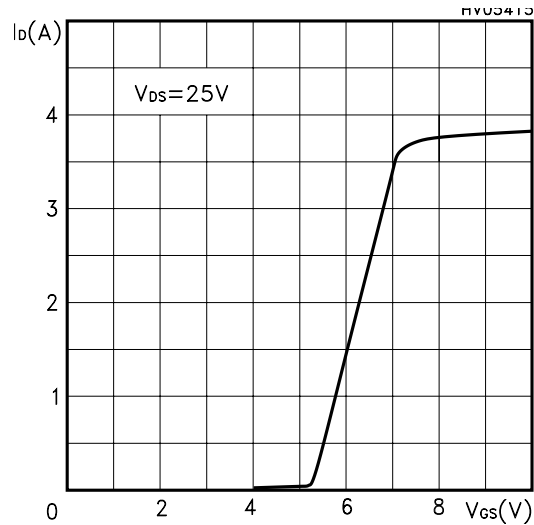
Thermal Impedance for TO-220FP



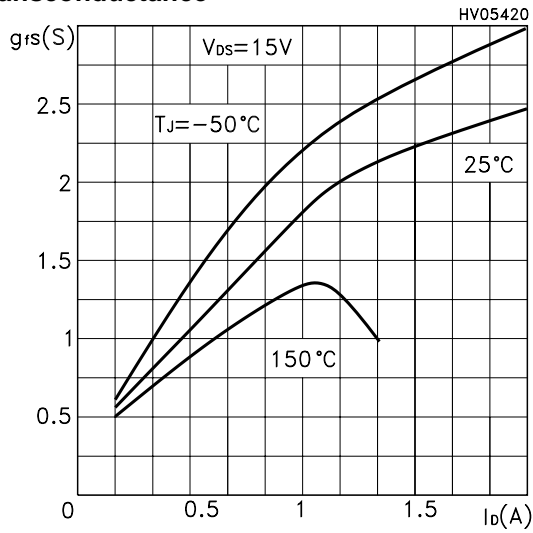
Output Characteristics



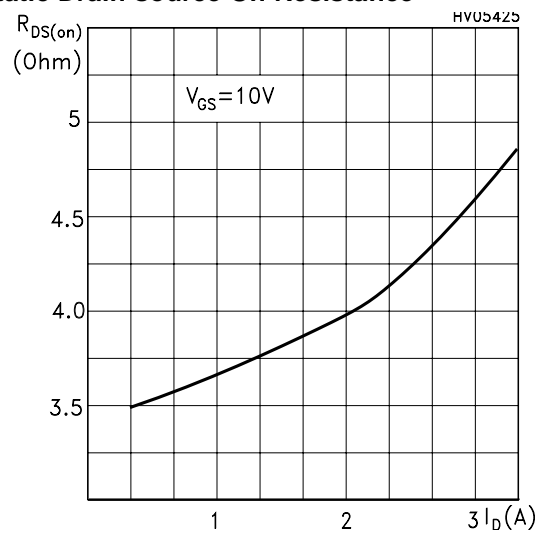
Transfer Characteristics



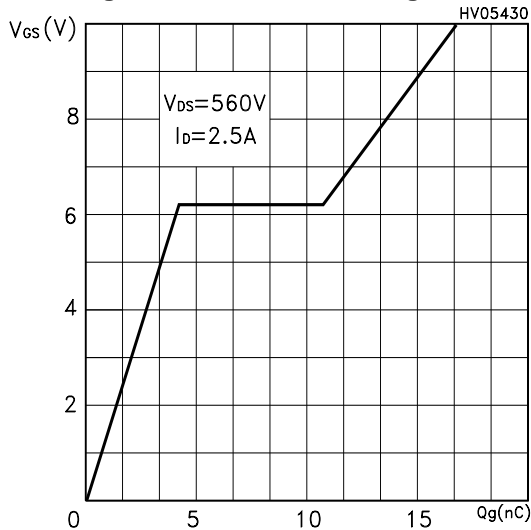
**Transconductance**



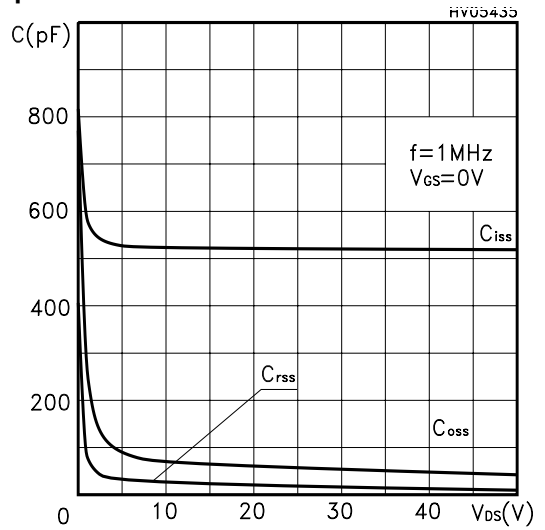
**Static Drain-source On Resistance**



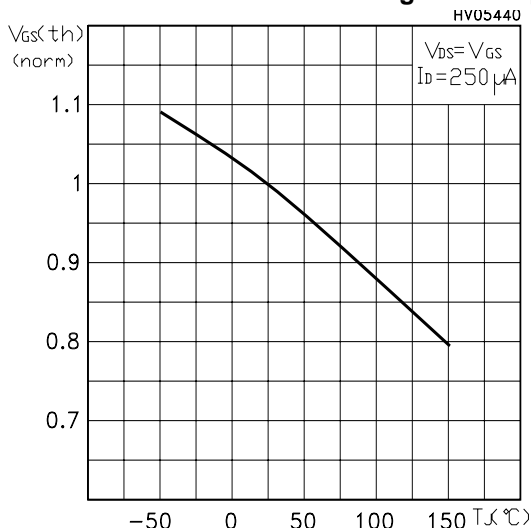
**Gate Charge vs Gate-source Voltage**



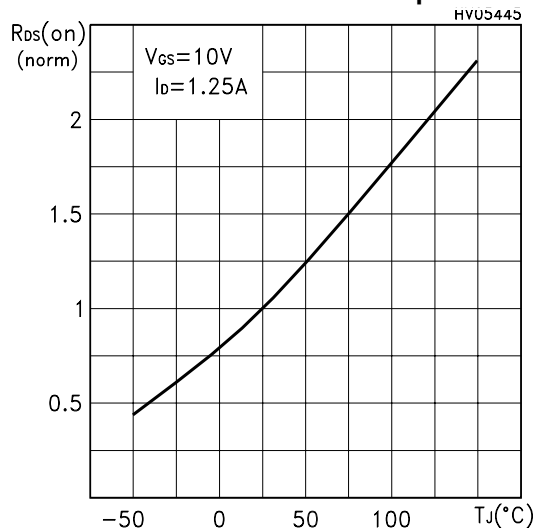
**Capacitance Variations**



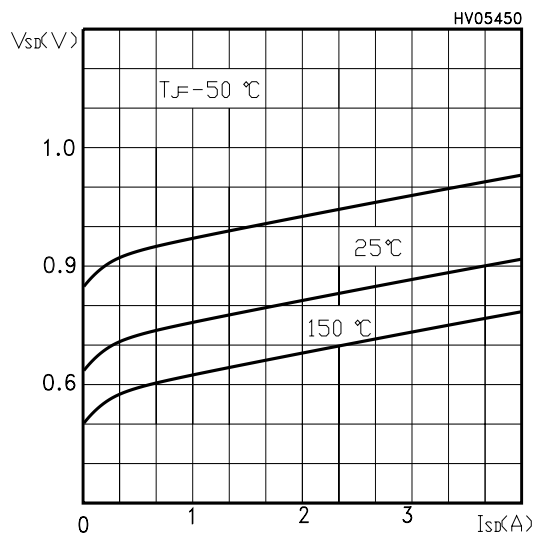
**Normalized Gate Threshold Voltage vs Temp.**



**Normalized On Resistance vs Temperature**



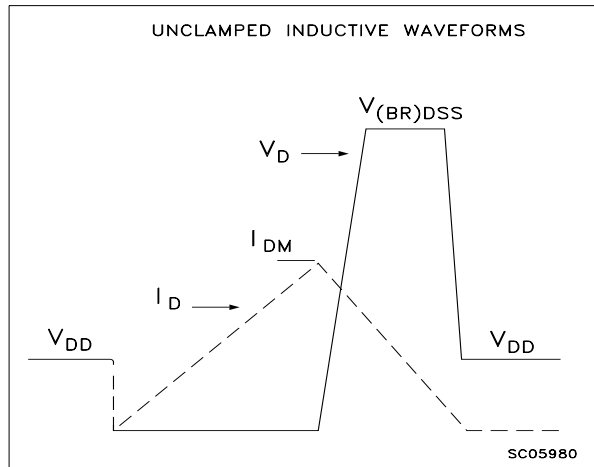
Source-drain Diode Forward Characteristics



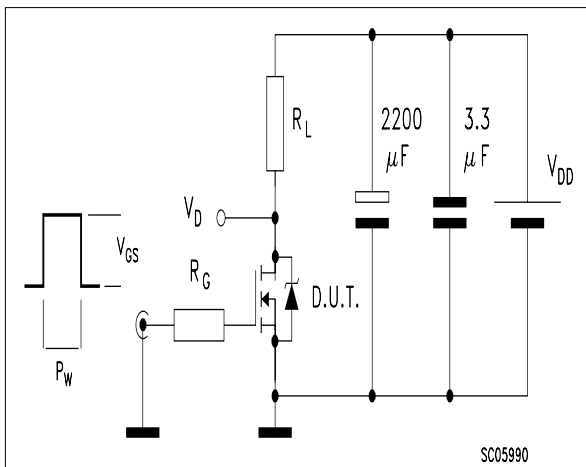
**Fig. 1: Unclamped Inductive Load Test Circuit**



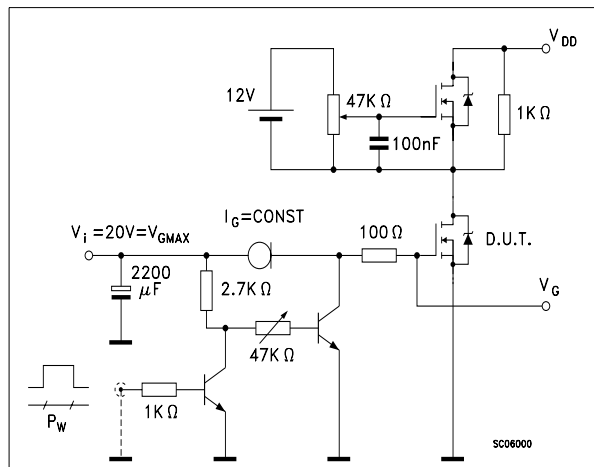
**Fig. 2: Unclamped Inductive Waveform**



**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

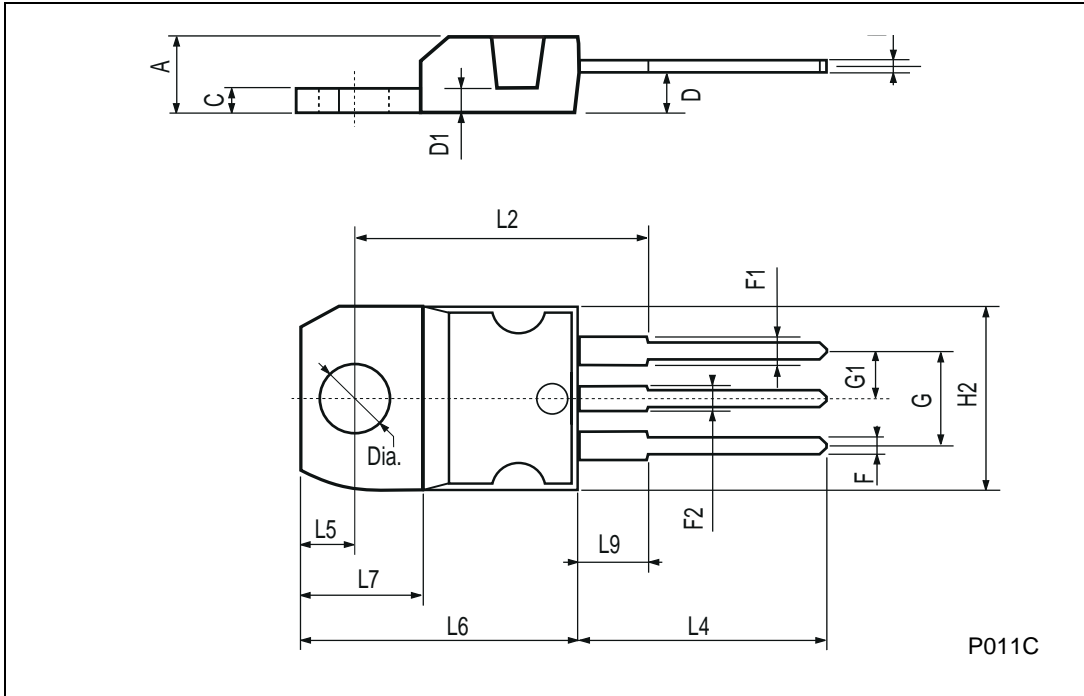


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



**TO-220 MECHANICAL DATA**

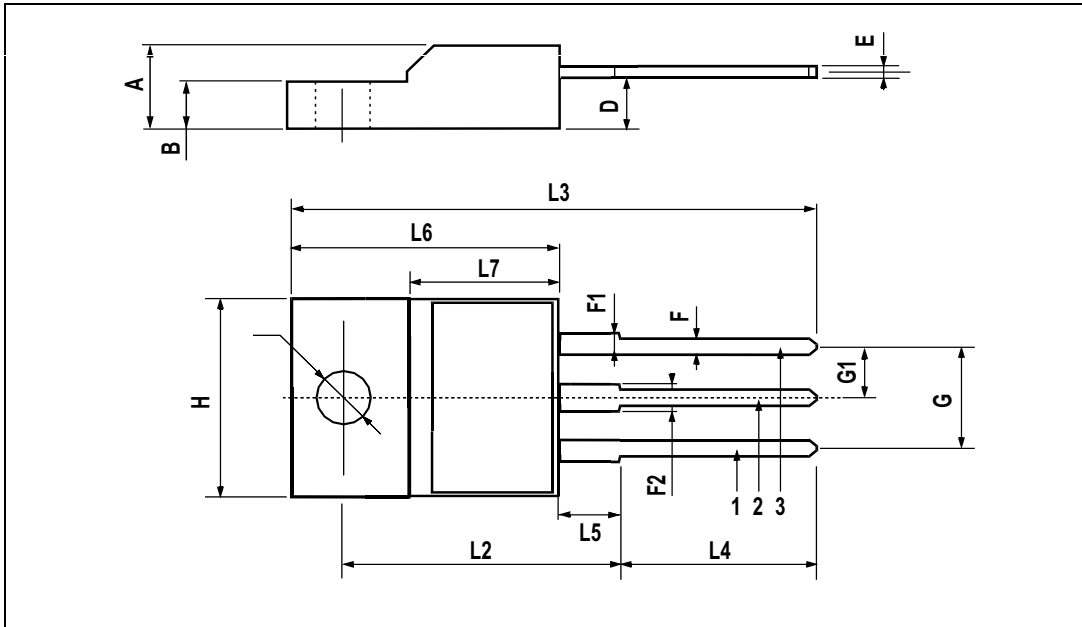
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151





**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -  
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>